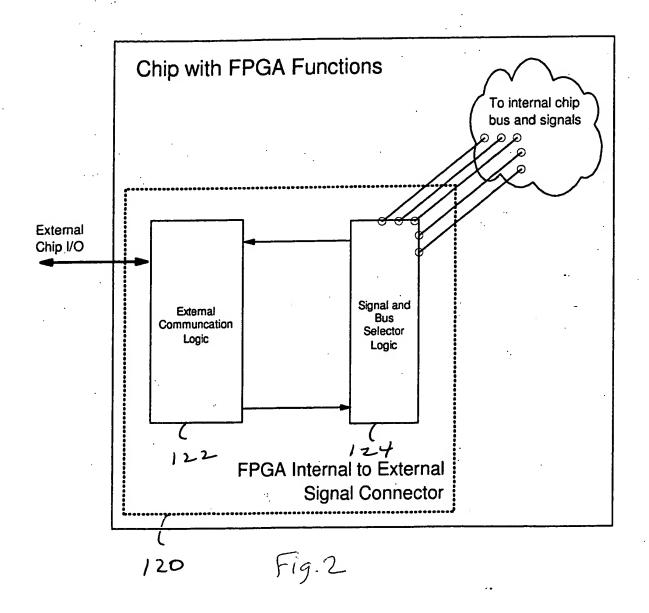


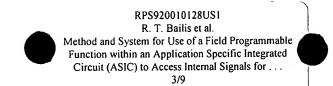
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Fig. 1

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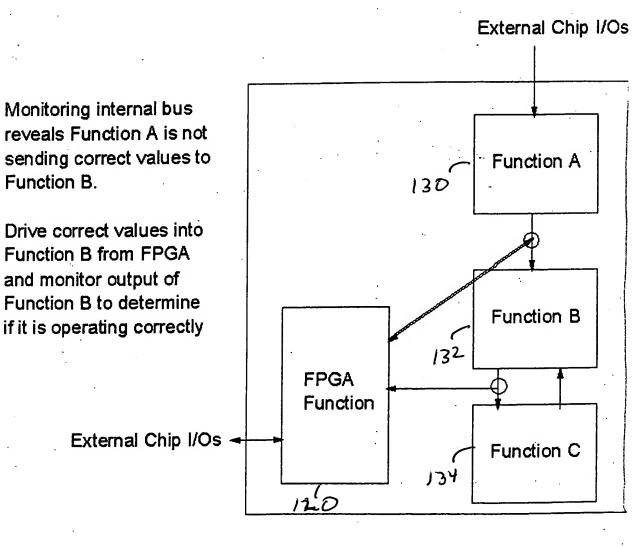
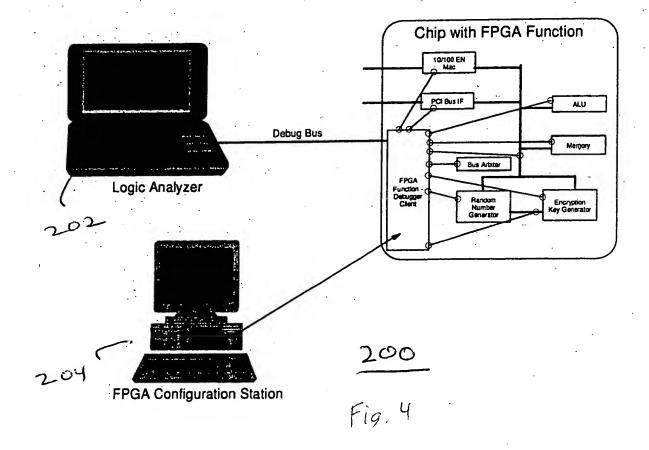


Fig. 3

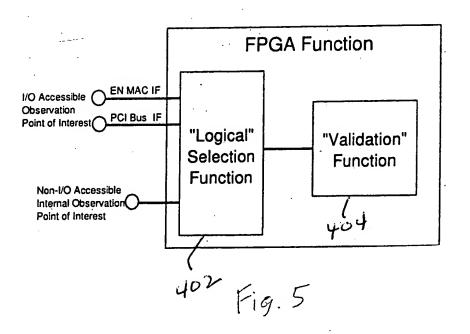
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- Memory and Memory Bus Debug
- MAC Bus Debug
- PCI, Internal Bus and Bus Arbiter Debug
- Processor Debug
- Clock and Clock Distribution Debug

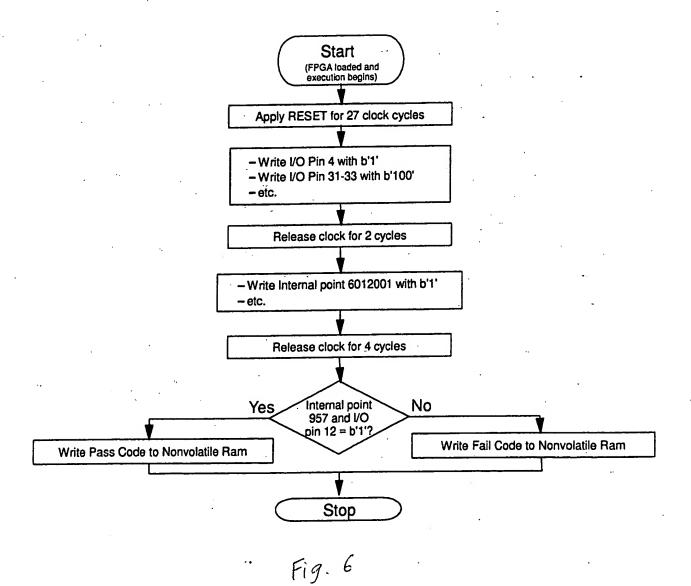


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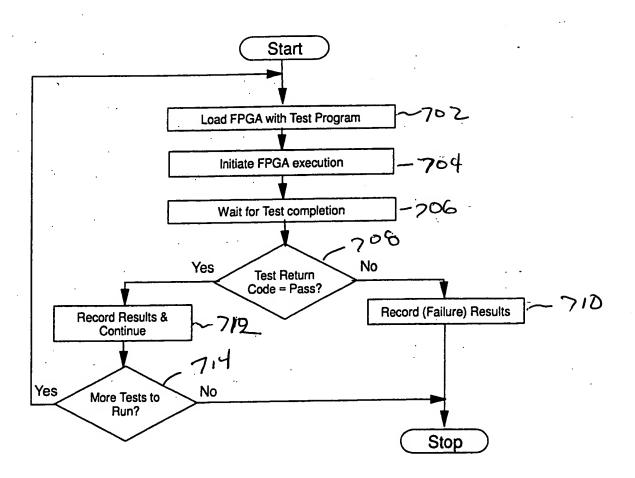
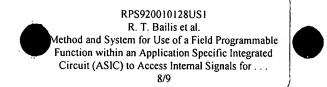


Fig. 7



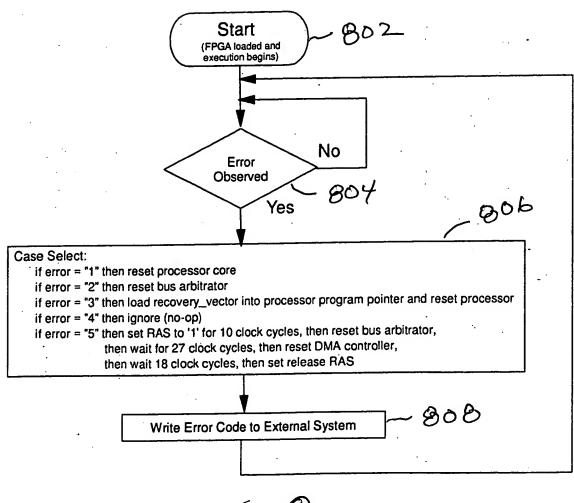


Fig. 8

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Function within an Application Specific Integral

Circuit (ASIC) to Access Internal Signals for . . .

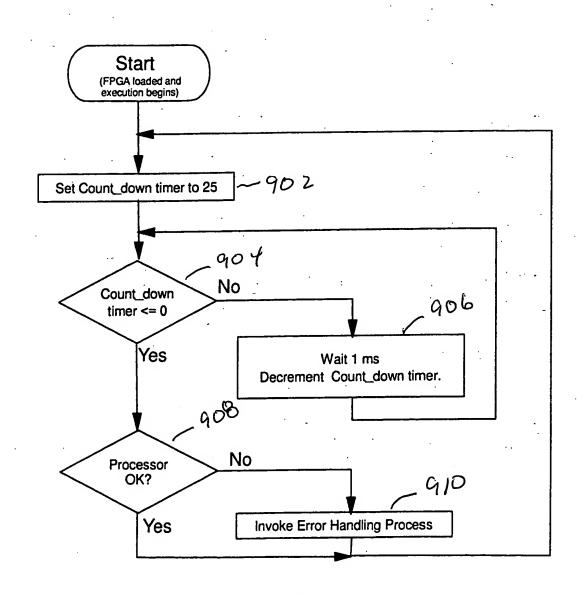


Fig. 9